WHAT IS CLAIMED IS:

1. A digital bus monitor device for observing data on a bus connected to a plurality of devices comprising:

input circuitry for receiving data from the bus;

test circuitry connected to said input circuitry for storing data in response to a predetermined condition while the devices are in a functioning mode.

2. The digital bus monitor of Claim 1 wherein said test circuitry comprises:

event qualification circuitry connected to said input circuitry to indicate when said predetermined condition has occurred.

3. The digital bus monitor of Claim 2 wherein said test circuitry further comprises an expected data memory for storing a plurality of expected data words associated with said predetermined condition.

4. The digital bus monitor of Claim 3 wherein said test circuitry is operable to compare said expected data word with data words received from said circuitry and is operable to indicate whether said received data matches said expected data word.

5. The digital bus monitor of Claim 4 wherein said test circuitry further comprises a masking data memory for storing a masking data word associated with said expected data word, said masking data word identifying portions of said expected data word where matching is not required for a matching indication.

6. The digital bus monitor of Claim 2 wherein said test circuitry is operable to perform signature analysis on said incoming data from the bus in response to said predetermined condition.

7. The digital bus monitor of Claim 6 wherein said test circuitry is further operable to selectively mask portions of said incoming data from the bus to identify the source of an error after an incorrect signature has been detected.

8. The digital bus monitor of Claim 5 wherein said expected data memory comprises a plurality of memory locations for storing respective expected data words.

9. The digital bus monitor of Claim 1 and further comprising scan path circuitry for serially transferring data stored in the monitor to an external controller for inspection.

10. The digital bus monitor of Claim 1 wherein said test circuitry further comprises a test memory buffer to store a plurality of data words from the bus responsive to said predetermined condition.

11. The digital bus monitor of Claim 10 wherein said test memory buffer is operable to store a plurality of data words contemporaneously with signature analysis being performed on said plurality of data words by said test circuitry.

12. The digital bus monitor of Claim 2 wherein said event qualification circuitry is operable to receive clock signals from one of a plurality of sources.

13. The digital bus monitor of Claim 1 wherein said testing circuitry is operable to start storing data in response to a first predetermined condition and operable to stop storing data in response to a second predetermined condition.

14. The digital bus monitor of Claim 13 wherein said testing circuitry is operable to resume storing data after a third predetermined condition and stop storing data after a fourth predetermined condition.

15. The digital bus monitor of Claim 1 wherein said test circuitry comprises:

control circuitry to store data responsive to a selected protocol a predetermined number of times; and

counter circuitry to count the number of storage operations responsive to the protocol.

16. The digital bus monitor of Claim 1 wherein said digital bus monitor further comprises cascade circuitry for cascading a plurality of digital bus monitoring devices.

17. A method of testing data transfers on a bus connected between a plurality of devices comprising the steps of:

receiving incoming data from the bus;

detecting the occurrence of a predetermined condition; and

processing input data in response to said predetermined condition while the integrated circuit is in the functioning mode.

18. The method of Claim 17 wherein said step of detecting the predetermined condition comprises the step of comparing said incoming data with predetermined expected data.

19. The method of Claim 17 wherein said processing step comprises the step of performing signature analysis on said incoming data.

20. The method of Claim 19 and wherein said processing step further comprises the step of storing said incoming data in a memory buffer contemporaneously with said step of signature analysis.

21. The method of Claim 19 and wherein said processing step further comprises the step of selectively masking one or more of the bits of said incoming data.

22. The method of Claim 17 wherein said step of processing data comprises the step of storing data in sequential locations in a memory buffer.

23. The method of Claim 22 and further comprising the step of ceasing to process said incoming data in response to a second predetermined condition.

24. The method of Claim 23 and further comprising the step of resuming processing of incoming data in response to a third predetermined condition.